Government of Karnataka
DEPARTMENT OF TECHNICAL EDUCATION

Program	**Electronics and Communication Engineering**	**Semester**	**III**
Course Name	**Digital Electronics-II**	**Type of Course**	Integrated
Course Code	**25EC31I**	**Contact Hours**	08 Hours/week 104 Hours/Sem
Teaching Scheme	L: T:P: 4:0:4	**Credits**	06
CIE Marks	**50**	**SEE Marks**	**50 (Theory)**

1. **Rationale:**

Digital electronics emphasizes the design and analysis of circuits using Boolean algebra, logic gates, and sequential logic. This encourages students to develop strong problem-solving skills, as they must translate complex real-world problems into solvable logic models. These skills are transferable to many fields of study and career paths.

As emerging technologies such as the Internet of Things (IoT), artificial intelligence (AI), machine learning (ML), and autonomous systems continue to grow, knowledge of digital electronics becomes crucial. These technologies often require highly efficient, specialized digital circuits and systems to process and communicate data in real-time.

The demand for professionals skilled in digital electronics is high across industries such as semiconductor manufacturing, telecommunications, consumer electronics, automotive, aerospace, and defense. Understanding digital circuits opens up a wide range of career opportunities, from circuit design and verification to embedded system development and hardware-software integration.

2. **Course Outcomes:** At the end of the Course, the student will be able to:

CO 1	Construct, analyze and verify the functioning of simple digital circuits/ICs using suitable Electronic design automation (EDA) tools.
CO 2	Design a sequential circuit for a specific application and test the circuit to obtain the desired result/output
CO 3	List the various types of A to D, D to A converters along with memory and for a specific application select the appropriate converters and/or memory types to be used to obtain the specific result/output
CO 4	Comprehend the need of VLSI ,hardware description language (HDL) and its role in modern electronic applications.

3. Course Content.

Week	CO	PO	Theory	Practice
1	**1,2**	**1,4**	1. **Sequential Circuits:** Introduction to sequential circuits, applications. 2. Comparison between Combinational and Sequential circuits. 3. Basic concepts of clock pulses. Triggering (positive and negative level and edge triggered). 4. T_{on}, T_{off} and Duty cycle (2 different duty cycles), Periodic Time Interval, and timing diagrams.	1. Familiarization of lab view software with simple experiments (any two). 2. Familiarization of other open source software that can be used for simulation.
2	**1,2**	**1,3, 4**	1. **Flip flops**: Introduction and applications of Flip flops. 2. SR flip flop- Operation, Gate level circuit (NAND gates), Truth table, timing diagram. 3. JK flip flop- Operation, Gate level circuit (NAND gates), Truth table and timing diagram. 4. Race around condition – concept. steps to avoid race around conditions.	1. Verify the truth table of the following experiments using simulation software. i. SR Flip flop. ii. JK Flip flop. 2. Verify the truth table of the following experiments using Digital Trainer Kit. i. SR Flip flop (using NAND gates) ii. JK Flip flop (7476 IC)
3	**1,2**	**1,3, 4**	1. Master slave JK Flip flop – circuit diagram, working principle. 2. D Flip flop- Operation, Gate level circuit (NAND gates), Truth table and timing diagram. 3. T Flip flop- Operation, Gate level circuit (NAND gates), Truth table and timing diagram. **4.** Implement D and T flip flop using JK flip flop	1. Verify the truth table of the following experiments using simulation software. i. D flip flop. ii. T flip flop. 2. Verify the truth table of the following experiments using Digital Trainer Kit. i. D flip flop using JK flip flop. ii. T flip flop using JK flip flop.
4	**1,2**	**1,3, 4,5**	1. **Shift Registers** – concept, applications. Types of Shift Registers –SISO - block diagram, working principle & truth table.	1. Verify the truth table of the following experiments using simulation software.

			2. SIPO - block diagram, working principle & truth table. 3. PISO - block diagram, working principle & truth table 4. PIPO - block diagram, working principle & truth table.	i. SISO shift registers. ii. PIPO shift registers. 2. Verify the truth table of the following experiments using Digital Trainer Kit with suitable IC's. i. SIPO shift registers. ii. PISO shift registers.
5	**1,2**	**1,3, 4,5**	1. **Counters** – concept, types, applications. 2. Concept of ripple, synchronous and asynchronous counters, Concept of up/down counters, Modulus counter. **3.** 3-bit asynchronous counter operation, truth table and timing diagram of up counters. **4.** 4 bit asynchronous counter operation, truth table and timing diagram of down counters.	1. Verify the truth table of the following experiments using simulation software. i. 3-bit Ripple counter. ii. Decade counter. 2. Verify the truth table of the following experiments using Digital Trainer Kit. i. 3-bit Ripple counter using 7476 IC. ii. Decade counter using IC7490.
6	**1,2**	**1,3, 4,5**	1. 3-bit Synchronous counter operation, truth table and timing diagram. 2. 4-bit Synchronous counter operation, truth table and timing diagram. 3. Mod N Counter-Mod 5 - operation, truth table. 4. Mod N Counter- Mod 8 - operation, truth table.	I Verify the truth table of the following experiments using simulation software. i. Ring counter ii. Johnson counter II Verify the truth table of the following experiments using Digital Trainer Kit with suitable IC's. i. Ring counter. ii. Johnson counter
7	**2,3**	**1,3, 5**	1. **Memories**: Classification of Memories, Comparison of ROM and RAM, 2. ROM – types (PROM, EPROM, EEPROM), applications. 3. EPROM- working principle. **4.** Comparison of ROM, PROM, EPROM	Illustrate the storing and retrieving of data in ROM using decoder & OR gates.(read and write operation)
8	**2,3**	**1,3, 5**	1. RAM – types, (static and dynamic RAM cells) working principle,	

			applications. 2. Comparison SRAM and DRAM. 3. Flash Memory- Operation and applications. 4. Features of SDRAM, DDRAM.	Illustrate the storing and retrieving of data in RAM using suitable IC. (read and write operation)
9	**2,3**	**1,3, 5**	1. **Data convertors**- concept and significance. **A/D converters-** concept, types, applications. 2. specifications-resolution, accuracy, non-linearity and conversion time. 3. Successive approximation ADC– block diagram, working principle. 4. Identify ADCs IC's and list their features.	i. Construct/Simulate and verify the working of 3-bit flash ADC. ii. Interpret the data sheets of ADC IC's (any two). List the alternate IC's that perform similar operation.
10	**2,3**	**1,3, 4,5**	1. **D/A converters-** concept, types, and applications. 2. specifications- resolution, accuracy, settling time, speed, linearity and monotonicity. 3. R-2R Ladder DAC – block diagram, working principle. 4. Identify DAC IC's and list their features.	i. Construct/Simulate and verify the working of 4-bit weighted resistor DAC. ii. Interpret the data sheets of DAC IC (any two). List the alternate IC's that perform similar operation.
11	**1,2 ,3**	**1,3, 4,5**	1. Introduction to PLDs- PAL, PLA, CPLD, FPGA, ASIC. 2. PAL- block diagram, components, applications. 3,4. Implementation of Boolean expressions using PAL (any two).	i. Implement a combinational with 3-Inputs and 2-Outputs using PAL in simulation software. ii. Implement the following Boolean expression using PAL, F1= $\sum$ m (3,5,7) and F2 = $\sum$ m (4,5,7).
12	**1,2 ,3**	**1,3, 4,5**	1. PLA- block diagram, components, applications. 2. Comparison between PAL & PLA. 3,4. Implementation of a Boolean expressions using PLA (any two).	i. Implement full adder circuit using PLA in simulation software. ii. Implement a 3 bit binary-to-Gray code converter using PLA.

13	**1,3 ,4**	**1,4, 5,7**	1. CMOS Inverter – schematic diagram & operation. 2. VLSI – concept, significance, applications. 3,4 Hardware Description Languages(HDL) – types, comparison between VHDL & Verilog, applications.	i. Construct/Simulate and verify the working of CMOS Inverter. ii. List the simulation software's (EDA tools) used for digital design of VLSI circuits.

Note:

1. In practice sessions all video demonstrations should be followed by MCQ/Quiz/ Subjective questions and evaluation has to be documented.

2. Online course completion certification to be done on relevant topics on Swayam/NPTEL/Infosys Springboard platforms or any other platform.

3. Problems statement to be collected from the relevant industries, resolve and submit it to the course coordinator.

4. References:

a. Digital principles and applications. Donald P Leach, Albert Paul Malvino, Goutam Saha, McGraw Hill Publisher, 8th edition, ISBN 10: 9339203402 ISBN 13: 9789339203405

b. Digital Systems-principles and applications. Ronald J. Tocci, Neal S.Widmer, Gregory L.Moss, 10th edition,ISBN : 0131725793

c. Digital Electronics –principles and integrated circuits. Anil K. Maini. Wiley publications,first edition . ISBN: 978-0-470-03214-5

d. Digital Computer Fundamentals, - Thomas C Bartee ,McGraw-Hill Publisher,6th edition.ISBN 10: 0070038996 / ISBN 13: 9780070038998

e. Digital fundamentals –Floyd and Jain, PEARSON EDUCATION publication, 8th Edition , ISBN-13: 978-0132359238 ,ISBN-10: 0132359235.

5. CIE Assessment Methodologies

Sl. No	**CIE Assessment**	**Test Week**	**Duration (minutes)**	**Max marks**	
1.	CIE-1 Theory Test	4	90	50	Average of all CIE=50 Marks
2.	CIE-2 Practice Test	7	180	50	
3	CIE-3 Theory Test	10	90	50	
4.	CIE-4 Practice Test	13	180	50	
5	CIE-5 Portfolio evaluation of all the activities through Rubrics	1-13		50	
				Total	**50 Marks**

Note:

Portfolio evaluation includes average of (a) and (b)

a) Any one of the suggested activity model with report and presentation / simulation evaluated for 50 marks.

b) Each laboratory exercise will be evaluated for a total of 50 marks. The evaluation will include the following components:

1. Written description of the experiment in the observation book.
2. Conducting the experiment and the associated learning outcomes.
3. The results obtained from the experiment.
4. Corrections and evaluations of the experiment completed in the previous class, documented in the record book.

6. SEE - Theory Assessment Methodologies.

Sl. No	SEE – Theory Assessment	Duration	Exam Paper Max marks	Exam Paper Max Marks scale down to (Conversion)	Min marks to pass
1.	Semester End Examination-Theory	3 Hours	100	50	20

7. CIE Theory Test model question paper.

Program	**Electronics and Communication Engineering**			Semester -III	
Course Name	**Digital Electronics-II**			Test	I/III
Course Code	**25EC31I**	**Duration**	90 min	Marks	50
Name of the Course Coordinator:					
Note: Answer any one full question from each section. Each full question carries equal marks.					

Q.No		Questions	Cognitive Level	Course Outcome	Marks
Section - 1					
1	i.	Given the circuit of a **ring counter**, analyze how the addition of a reset mechanism affects the stability and correctness of the counting sequence.	L3		10
	ii.	Explain the operation of S-R flip flop using NAND gates with its Truth Table	L3	CO 2	10
	iii.	Compare the functionality of a D flip-flop and a JK flip-flop. Under what conditions can they be considered equivalent?	L2		05
2	i.	Explain the operation of JK flip flop using NAND gates with its truth table.	L2		10
	ii.	How does the behaviour of an edge-triggered flip-flop differ from a level-triggered flip-flop? Analyse their impact on circuit performance.	L3	CO 2	10
	iii.	Illustrate the purpose of the preset and clear	L3		05

	inputs in a flip-flop.			
	Section 2			
3	a) Examine a shift register circuit that fails to produce the expected output. Identify the possible sources of error (e.g., clock issues, flip-flop malfunction, incorrect wiring).	L3	CO1	10
	b) Interpret the operation of SISO shift register with block diagram and truth table	L3		10
	c) Why are shift registers classified as sequential circuits rather than combinational circuits	L2		05
4	a) If one flip-flop in a shift register malfunctions (e.g., fails to hold data), how will this impact the overall operation of the circuit?	L3	CO 1	10
	b) Illustrate the operation of PISO shift register with its block diagram and truth table	L2		10
	c) Establish the usage of shift registers in digital counters.	L2		05

Note for the Course coordinator:

1. Each question may have one, two or three subdivisions. Optional questions in each section carry the same weightage of marks, cognitive level and course outcomes.
2. All questions must be framed under Understand (L2) & Apply (L3) cognitive level using Revised Bloom's Taxonomy.

Signature of the Course Coordinator | **Signature of the HOD** | **Signature of the IQAC Chairman**

8. CIE Practice Test model question paper

Program	**Electronics and Communication Engineering**			**Semester**	3
Course Name	**Digital Electronics-II**			**Test**	**II/IV**
Course Code	**25EC31I**	**Duration**	**180 min**	**Marks**	**50**
Name of the Course Coordinator:					

Questions	CO	Marks
write up for 2 experiments & conduction of any one experiment.	2,3	**50**
Scheme of assessment **a) Writing the Circuit diagram, tabular column, calculations etc for two experiments.** **b) Rigup and conduction of any one** **c) Result/output** **d) Troubleshooting steps** **e) Viva-voce**		**20M** **10M** **05M** **05M** **10M**
Total Marks		**50 M**

Signature of the Course Coordinator | **Signature of the HOD** | **Signature of the IQAC Chairman**

9. Suggestive Activities for Tutorials:

The List is an Example and not inclusive of all possible activities of the course. Student and Faculty are encouraged to choose activities that are relevant to the topic.

Sl.No.	**Suggestive Activities for Tutorials**
01	Give a presentation on how counters can be used in a simple car parking system.
02	Mini project on implementation of footfall counter for various purposes in your institution.
03	Building an elevator controller system using sequential circuits.
04	Developing a digital clock with programmable features.
05	Designing a simple CPU or a memory controller.
06	Study the latest technological changes in VLSI and present the impact of these changes on industry.
07	Prepare a block diagram approach to construct a digital clock or a frequency counter or a digital voltmeter or any other similar digital electronic circuits and analyze the cost of the application

10. Rubrics for Assessment of Activity (Qualitative Assessment)

Sl. No.	Dimension	Beginner	Intermediate	Good	Advanced	Expert	Students Score
		10	20	30	40	50	
1		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	40
2		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	30
3		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	50
4		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	20
	Average Marks=(40+30+50+20)/4=35						**35**

Note: Dimension and Descriptor shall be defined by the respective course coordinator as per the activities

11. **Equipment/software list with Specification for a batch of 30 students.**

Sl.No.	Particulars	Quantity
1	Digital Trainer Kits	15
2	Dual trace oscilloscope. – CRO. (20MHz)	15
3	Digital mustimeters	10
4	ICs - 7400,7402,7404,7408,7432,7486,7442,7445,7446,7474,7476,7427,7489, 7490,7494,7495,74141,74148,74153,74157,74155,74193,74194, DAC0808, ADC-0800,741,	20 each
5	Patch cards(different lengths)	300
6	Digital IC Tester	5
7	Computers	15
8	Free simulation software	